FIG. 4 is a schematic of a signal analyzer constructed in accordance with a preferred embodiment of the invention. Input 61 is coupled to the output of D-flip-flop 31 (FIG. 2), input 62 is coupled to the output of D-flip-flop 32 (FIG. 2), and input 63 is coupled to the output of D-flip-flop 33 (FIG. 2). Inputs 61 and 62 are coupled to AND gate 65, which produces a logic "1" when the received signal (line input) is greater than the microphone signal and is greater than a predetermined threshold. The output of AND gate 65 is coupled to the "down" input of accumulator 40. Inverted input 62 and input 63 are coupled to AND gate 66, which produces a logic "1" when the received signal (line input) is less than a predetermined threshold and the microphone signal is greater than a predetermined threshold. The thresholds need not be the same value. The output of AND gate 66 is coupled to the "up" input of accumulator 40.

In the claims:

Kindly amend claims 1 and 2 as follows.

1 (Amended). A method for comparing two electrical signals, said method comprising the steps of:

(a) comparing the signals to each other and to at least one threshold to produce a binary representation of the comparisons;

(b) converting a plurality of binary representations into a first count; and

(c) comparing the first count to at least one count threshold.

2 (Amended). The method as set forth in claim 1 wherein comparing step (a) includes the steps of:

comparing the signals in an analog comparator;

sampling the output of the comparator to produce said binary representation of the comparison.

REMARKS

Reconsideration of the above-identified application is respectfully requested.

The objection to the disclosure is believed overcome by the foregoing amendment. Other typographical errors were also corrected.